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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,421	03/26/2004	Jin Ki Kim	PAT 980-2	7842

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BORDEN LADNER GERVAIS LLP
WORLD EXCHANGE PLAZA
100 QUEEN STREET SUITE 1100
OTTAWA, ON K1P 1J9
CANADA

EXAMINER	
HUR, JUNG H	
ART UNIT	**PAPER NUMBER**
2824	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/809,421	KIM, JIN KI	
	Examiner	Art Unit	
	Jung (John) H. Hur	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 7-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 7-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 28 February 2007 has been entered.

It is noted that **THIS ACTION IS MADE FINAL** (see comments below in the Conclusion section).

Applicant's Remarks

2. Acknowledgment is made of applicant's submission, filed 28 February 2007. The remarks disclosed therein have been considered.

No claims have been added or cancelled by said submission. Therefore, claims 1-4 and 7-28 are pending in the application.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 7, 8, 10, 15-17 and 24-28 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Pat. No. 6,697,276 (Pereira et al.) in view of admitted prior art ("Admission").

Regarding claim 1, Pereira discloses a hybrid content addressable memory (CAM) array comprising: a first memory portion (each row including a number of ternary CAM cells; see column 34, lines 19-23) having a first type of content addressable memory cells (ternary CAM cells) arranged in rows and columns (as implied by 601 in Fig. 42, as a reference); a second memory portion (each row including a number of binary CAM cells; see column 34, lines 19-23) having a second type of content addressable memory cells (binary CAM cells) arranged in rows and columns, the second type of content addressable memory cells being electrically coupled to the first type of content addressable memory cells (since they are part of each row), the second memory portion being operable simultaneously with the first memory portion (since they are part of each row).

Pereira does not expressly disclose that each of the first type of content addressable memory cells include search and compare stacks for coupling a matchline to a tail line if search data matches stored data, and each second type of content addressable memory cell is smaller in size than each first type of content addressable memory cell.

Admission, for example in Figs. 3-5, discloses a first type of content addressable memory cells (ternary type of Fig. 3 or 4, for example) including search and compare stacks (including 54-60) for coupling a matchline (ML) to a tail line (TL) if search data matches stored data, and a second type of content addressable memory cell (binary type of Fig. 5) that is smaller in size than

the first type of content addressable memory cell (since, in the binary cell of Fig. 5, only one SRAM cell is used, as opposed to two SRAM cells in the ternary cell of Fig. 3 or 4).

Since Pereira does not disclose the specifics of the ternary and binary CAM cells, it would have been obvious at the time the invention was made to a person having ordinary skill in the art, in view of Admission, to use the ternary and binary CAM cells of Admission for the ternary and binary CAM cells of Pereira, with each second type of content addressable memory cell being smaller in size than each first type of content addressable memory cell, since such ternary and binary CAM cells were common and well known in the art as exemplary ternary and binary CAM cells (as disclosed in Admission).

Regarding claims 2, 3, 10, 15 and 16, the above combination further discloses that the first memory portion and the second memory portion include matchlines (associated with each row, as disclosed in Pereira, column 34, lines 19-23), each matchline of the first memory portion being coupled to the first type of content addressable memory cells (the portion of the matchline of each row for the ternary cells), and each matchline of the second memory portion being coupled to the second type of content addressable memory cells (the portion of the matchline of each row for the binary cells);

wherein the first type of content addressable memory cells include ternary content addressable memory cells and the second type of content addressable memory cells include binary content addressable memory cells (see Pereira, column 34, lines 19-23);

wherein the first type of content addressable memory cells and the second type of content addressable memory cells of a row are coupled to a logical matchline (the matchline associated with each row, as disclosed in Pereira, column 34, lines 19-23).

Regarding claims 7, 8 and 17, the above combination further discloses that the CAM cells include SRAM based CAM cells (see Admission, Figs. 3-5).

Regarding claims 24-28, the above combination further discloses

that each search and compare stack includes a compare transistor (for example, 54 in Fig. 4 of Admission) and a search transistor (56) serially connected between the matchline and the tail line (see Fig. 4), the compare transistor gate receiving the stored data (from 42) and the search transistor gate receiving the search data (SLb);

a second compare transistor (for example, 58 in Fig. 4 of Admission) and a second search transistor (60) serially connected between the matchline and the tail line (see Fig. 4), the second compare transistor gate receiving complementary stored data (from 42) and the second search transistor gate receiving complementary search data (SL);

that the stored data includes a first data bit (that of 42 in Fig. 3 or 4 of Admission) and a second data bit (that of 44), the search data includes a first search bit (SLb) and a second search bit (SL);

that the search and compare stack includes a first compare transistor (54 in Fig. 3 of Admission) and a first search transistor (56) serially connected between the matchline and the tail line (see Fig. 3), and a second compare transistor (58) and a second search transistor (60)

serially connected between the matchline and the tail line (see Fig. 3), the first compare transistor gate receiving the first data bit (from 42), the second compare transistor gate receiving the second data bit (from 44), the first search transistor gate receiving the first search bit (SLb), and the second search transistor gate receiving the second search bit (SL);

that the search and compare stack includes a first compare transistor (54 in Fig. 4 of Admission), a first search transistor (56), and a mask transistor (72) serially connected between the matchline and the tail line (see Fig. 4), and a second compare transistor (58), a second search transistor (60), and the mask transistor (72) serially connected between the matchline and the tail line (see Fig. 4), the first compare transistor gate receiving the first data bit (from 42), the second compare transistor gate receiving a complement of the first data bit (from 42), the first search transistor gate receiving the first search bit (SLb), the second search transistor gate receiving the second search bit (SL), and the mask transistor receiving the second data bit (from 44).

5. Claims 4, 14 and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,697,276 (Pereira et al.) in view of admitted prior art ("Admission") as applied to claims 1-3 above, and further in view of U.S. Pat. No. 6,252,789 (Pereira et al.).

Regarding claims 4, 14, 21 and 22, the above Pereira/Admission combination discloses a hybrid content addressable memory (CAM) array as in claims 1-3 above, with the exception of the matchlines of the first memory portion and the matchlines of the second memory portion being interleaving with each other, or the first type of CAM cells and the second type of CAM cells of a column being coupled to common searchlines.

Pereira '789, for example in Fig. 22, discloses a data word chain (for example, 2210, representing a CAM entry unit) stored in more than one row of a CAM (for example, four rows of 2214; see Fig. 22).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to modify the CAM array of the above Pereira/Admission combination such that hash index CAM entries for a specific application requiring a number of binary CAM cells and a number of ternary CAM cells (as disclosed in Pereira '276, column 34, lines 19-23) would be represented by and stored in more than one row of a CAM (as in Pereira '789), resulting in first and second types of cells in a column having common searchlines and interleaved matchlines, for the purpose of effectively storing and searching CAM entries with a larger width than that of a CAM (see for example Pereira '789, column 1, lines 19-25 and 46-48).

Regarding claim 23, the above combination further discloses that the CAM cells include SRAM based CAM cells (see Admission, Figs. 3-5).

6. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,697,276 (Pereira et al.) in view of admitted prior art ("Admission") as applied to claim 1 above, and further in view of Voelkel (U.S. Pat. No. 6,108,227).

Regarding claim 9, the Pereira/Admission combination discloses a hybrid content addressable memory (CAM) array as in claim 1 above, with the exception of at least one of the first and the second type of CAM cells including configurable ternary-binary CAM cells.

Voelkel discloses configurable ternary-binary CAM cells (Fig. 2, with arrangements in which one or more columns can be switched between modes, or a switching capability can be performed for portions of an array; see column 7, lines 5-15).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to have at least one of the first and the second type of CAM cells of the Pereira/Admission combination include configurable ternary-binary CAM cells (such as that of Voelkel), for the purpose of increasing the configuration flexibility without increasing the overall CAM size (see for example Voelkel column 4, lines 21-33).

7. Claims 11-13 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pat. No. 6,697,276 (Pereira et al.) in view of admitted prior art ("Admission") as applied to claims 10 and 15 above, and further in view of Pereira (U.S. Pat. No. 6,191,970).

The above combination of Pereira '276 and Admission discloses a hybrid content addressable memory (CAM) array as in claims 10 and 15 above, with the exception of the logical matchline including a first matchline segment and a second matchline segment (or at least two matchline segments), wherein the first type of CAM cells are coupled to the first matchline segment and the second type of CAM cells are coupled to the second matchline segment.

Pereira '970, for example in Fig. 4, discloses a logical matchline (including ML_row) including a first matchline segment (ML_a) and a second matchline segment (ML_b) for a row of CAM cells (CAM CELLs in Fig. 4).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to segment the CAM cells and therefore the row matchline of Pereira

'276 into at least two segments, as in Pereira '970, such that, as a reasonable arrangement in light of Pereira '276, the ternary type CAM cells would be coupled to a first matchline segment and the binary type CAM cells would be coupled to a second matchline segment, for the purpose of reducing power consumption associated with precharging matchlines during compare operations (see for example Pereira '970, column 1, line 65 through column 2, line 2).

Response to Arguments

8. Applicant's arguments filed 28 February 2007 have been fully considered but they are not persuasive.

Regarding claims 1 and 15, Applicant argues, starting in the middle of page 2, that Pereira "does not discuss or infer a desire to conserve memory array space of the CAM device" and that "a person skilled in the art would not resort to using binary and ternary CAM cells of differing sizes, and will instead use CAM memory cells operable as both a ternary CAM cell and a binary CAM cell, as taught by Voelkel."

In response, since Pereira discloses that "each row within the ternary CAM device could include a number of binary CAM cells and a number of ternary CAM cells according to application needs" (column 34, lines 19-23) but does not expressly disclose any particulars of these binary and ternary CAM cells, one of ordinary skill in the art, in an effort to make and use Pereira's invention, would use conventional binary and ternary CAM cells (such as those of the admitted prior art, which were common and well known in the art) in each row according to application needs, as disclosed in column 34, lines 19-23 of Pereira. Further, it is noted that the outstanding rejection of at least claims 1 and 15 is not based on the Voelkel reference.

Applicant further argues, starting at the bottom of page 2, that Pereira "does not explicitly state that both the binary CAM cells and ternary CAM cells are simultaneously operable" and "does not state whether these are logical rows or physical rows" (top of page 3), and that "Hata...discloses a configuration where ternary and binary CAM storage capability are provided, however they cannot be simultaneously operated."

In response, in the context of the paragraph in which the statement "each row within the ternary CAM device could include a number of binary CAM cells and a number of ternary CAM cells according to application needs" is found (i.e., the paragraph of column 34, lines 1-23), Pereira discloses such row with both binary and ternary CAM cells as an alternative to a row with all ternary CAM cells, which in itself is disclosed as an alternative to a row having binary CAM cells (see for example column 34, lines 5-12 and 16-20), in which the whole row is operated simultaneously to compare with the inputted hash index (see for example Fig. 42 of Pereira). Therefore, the binary and ternary CAM cells in each row as disclosed in column 34, lines 19-23 of Pereira, would be operated simultaneously, as recited in claims 1 and 15. Further, it is noted that the outstanding rejection of at least claims 1 and 15 is not based on the Hata reference.

It is noted that, after further consideration, the 103 rejection of claims 4, 14 and 21-23 have been withdrawn, and a new ground of rejection is made in view of newly found prior art reference. See the rejection above.

Conclusion

9. All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) H. Hur whose telephone number is (571) 272-1870. The examiner can normally be reached on M-F 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

jhh

3/10/07

JUNG (JOHN) H. HUR
PRIMARY PATENT EXAMINER